Please amend the subject application as follows:

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 13, line 14 and ending at page 14, line 4 as follows:

--Fig. 2 shows a signal timing diagram 200 representing operation of the pixel circuit 100 for faster V_t compensation. Frame time period 201 is divided into write V_t time period 202, write data time period 203 and expose time period 204. The frame time period 201 is the time between time 205 and time 208. The write V_t time period 202 is the time between time 205 and time 206. The write data time period 203 is the time between time 206 and time 207. The expose time period 204 is the time between time 207 and time 208. A second frame time period starts at the end of a first frame time period. Typically, frame time period [[101]] 201 may be approximately 16.7 milliseconds. The write data period 203 and the expose time period 204 each may be approximately 8.3 milliseconds. While dependent upon TFT mobility, TFT channel width to length ratios, data storage capacitance, circuit voltages and desired accuracy, the write V_t period 202 may be approximately 0.1 to 0.2 milliseconds.--